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Low-Cost Lattice Matching Zn(Se)Te/Si Composite Substrates for HgCdSe and Type-2 Superlattices

by Yuanping Chen

ARL-TR-6642 **September 2013**

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14. ABSTRACT
Growth of ZnTe on Si using molecular beam epitaxy (MBE) has been pursued as a new approach for a lattice-matched, large-area, low-cost alternate substrate for both II-VI and III-V compound semiconductors with lattice constants very near 6.1 Å, such as HgCdSe and GaSb-based type-II strained-layer superlattices. In this report, we present our findings on the systematic studies of MBE growth parameters for both ZnTe(211) on Si(211) and ZnTe(100) on Si(100). Optimal MBE growth procedures have been established for producing ZnTe/Si wafers with high crystallinity, low defect, and etch pits densities, as well as excellent surface morphology. Using this baseline MBE growth process, we obtained 3-in ZnTe(211)/Si and ZnTe(100)/Si wafers with X-ray full-width at half-maximum (FWHM) as low as 70 and 103 arcsec, respectively.

15. SUBJECT TERMS
ZnSeTe, Si, HgCdSe, ZnTe, MBE, LWIR, defects, IR II-VI, Type-2 SLS

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1. Introduction

Infrared (IR) detectors and advanced IR focal-plane arrays (IRFPAs) were historically based primarily on HgCdTe grown on lattice-matched CdZnTe substrates, either by liquid phase epitaxy or molecular beam epitaxy (MBE). Due to the difficulties and cost associated with the fabrication of large-area CdZnTe wafers, there have been significant efforts to search for alternate substrates based on CdTe grown on either GaAs or Si (*1–5*). As a result, CdTe/Si grown by MBE has emerged as a viable alternate substrate, and MBE-grown HgCdTe on CdTe/Si has become a viable detector material for IRFPAs for mid-wavelength IR (MWIR) and short-wavelength IR (SWIR) applications (*6–8*). MWIR focal plane arrays (FPAs) made from HgCdTe/CdTe/Si, with array sizes as large as 1K × 1K and 2K × 2K, have been demonstrated by Teledyne Technologies Inc. and Raytheon Vision Systems, respectively. Despite these advances, however, challenges remain, especially for long-wavelength IR (LWIR) applications, due to the approximate two orders of magnitude increase in dislocation density for growth of HgCdTe on Si substrates, compared with HgCdTe grown on non-scalable CdZnTe substrates (*9*). It has been demonstrated that this higher dislocation level results in lower device performance, especially in the LWIR region (*10*). Thus, there is ongoing effort to either further reduce dislocations in HgCdTe/Si, or to render the dislocations electrically inactive (*11–14*).

In recent years, there has been renewed interest in exploring new IR materials based on type-II strained layer superlattices (T2-SLS) (*15, 16*) and HgCdSe (*17, 18*) alloys for LWIR applications. These compound semiconductor systems have lattice constants close to 6.1 Å and can be grown on closely lattice-matched, high quality and commercially available GaSb substrates. Although GaSb appears to be an optimal substrate, it does have some limitations, such as limited size (currently up to 4-in diameter) and relative expense (about \$88/cm^2), and the challenge of the growth of HgCdSe on GaSb, due to potential interface mixing and/or autodoping (*19–21*). Additionally, GaSb substrate technology is still maturing with high doping concentrations and relatively poorer polished surface morphologies with respect to Si, which presents additional challenges to the MBE growth of either T2-SLS or HgCdSe, in particular. Thus, it is desirable to develop an alternate low-cost and scalable substrate with lattice constant very near 6.1 Å, which can be tuned to lattice-match any configured T2-SLS system or HgCdSe alloys. For these reasons, we propose using ZnSeTe grown on Si as a composite substrate for both T2-SLS and HgCdSe. With the slight addition of Se into the ZnTe matrix, ZnSeTe can exactly match T2-SLS and HgCdSe lattices at any composition. In addition, ZnSeTe/Si is also lattice-matched to other important III-V and II-VI compound materials with lattice constants near 6.1 Å, as shown in figure 1. With the successful development of CdTe/Si as a alternate substrate for HgCdTe, in which thin ZnTe grown on Si is used as a buffer layer to bridge the lattice

parameter gap between Si and CdTe, we believe that high quality, thick ZnSeTe layers can be grown on Si, as well, and act as alternate substrates for both T2-SLS and HgCdSe, as well as other III-V and II-VI compound semiconductors near 6.1 Å. However, the growth of ZnSeTe on Si is highly challenging due to the large lattice mismatch (~12%) between Si and ZnSeTe. To date, the only research on ZnTe growth on Si has been related to the nucleation thin ZnTe buffer layer used for growing high quality CdTe/Si (*4*, *5*, *22*). To our knowledge, no work reported in the literature exists for high quality thick ZnTe/Si or ZnSeTe/Si.

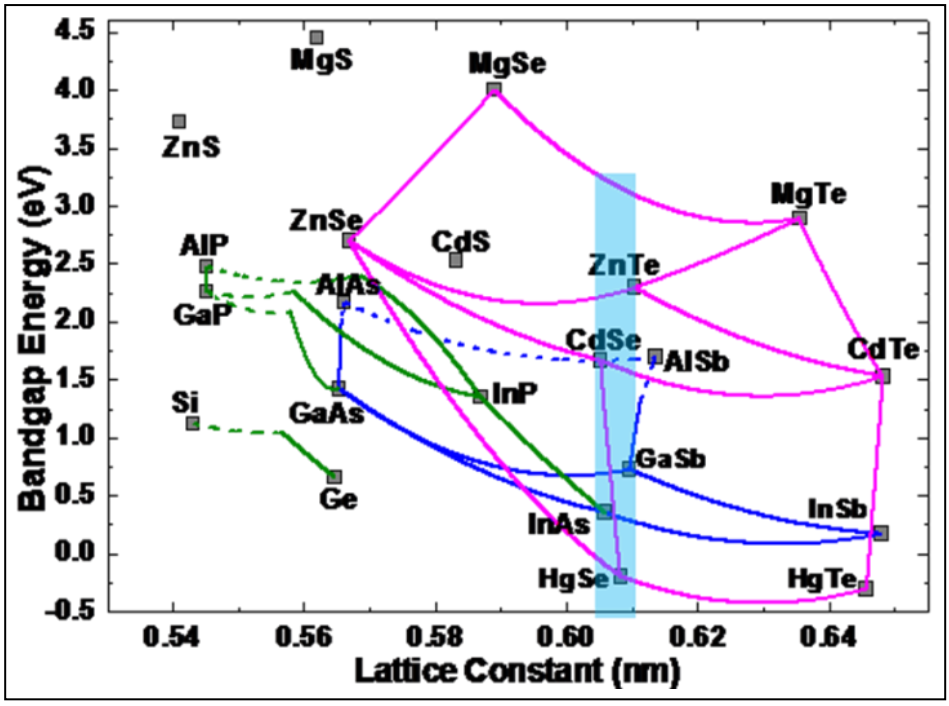

Figure 1. Energy gap versus lattice parameter for several semiconductor material systems.

We conducted systematic studies on the MBE growth of ZnTe on Si in both (211) and (100) orientations, aiming to establish a baseline growth process to obtain high quality ZnTe/Si substrates. For simplicity, we started with the growth of the binary ZnTe compound on Si. Lattice-matched ZnSeTe can then be obtained by adding a small percentage of Se while using the optimized growth process developed under these studies for ZnTe/Si, analogous to the successful growth of CdSeTe on Si by MBE using optimized growth process of CdTe on Si (*23*).

2. Experimental

2.1 Substrate Preparation

The substrates used for the growth are 3-in Si(100) wafers. The Si wafers were either lightly phosphor-doped or undoped with resistivity in the range of 10–50 ohm-cm. It is important to keep the resistivity above 10 ohm-cm to ensure the above 70% IR transmission in 1 to 12 micron spectrum range. P-type Si wafer tends to have higher IR absorption.

Before introduced into vacuum chamber, Si wafers were cleaned using a modified process based on conventional RCA process (*24*). The process is illustrated in following order:

1. Prepare five glass beakers and one plastic beaker with 1000 ml capacity. Fill plastic beaker with 950 ml de-ionized water (DIW) and 50 ml hydrogen fluride (HF) (49%) to make a dilute HF solution. Etch each glass beaker with the dilute HF solution and then rinse with DIW. The clean beakers were filled with DIW and set aside for later use.
2. Fill one glass beaker with 600 ml DIW, 120 ml ammonium hydroxide (NH_4OH), and 120 ml hydrogen peroxide (H_2O_2) (referred to as NH_4OH solution), and place the beaker on a hot plate.
3. Place the 3-in Si wafer onto a talon wafer holder. Blow the wafer surface with dry nitrogen gas to remove any dust particle attached to the surface. Insert the wafer into NH_4OH solution and heat for 30 min.
4. Use the plastic beaker to make a fresh dilute HF solution, as described in step 1.
5. Fill another glass beaker with 600 ml DIW and 120 ml hydrogen chloride (HCl) (37%) (referred to as HCl solution) and place the beaker on a hot plate.
6. Bring the beaker with the NH_4OH solution together with the Si wafer remaining submerged and place under running DIW until the liquid is at about room temperature.
7. Fill remaining three glass beakers with fresh DIW. Rinse the Si wafer in fresh DIW for seven consecutive bathes.
8. Add 120 H_2O_2 into the heated HCl solution.
9. Remove the Si wafer from DIW and submerge into prepared HF solution and etch for 100 s to strip native oxide from Si surface.

10. At the end of etching, slowly remove the Si wafer from HF solution (wafer will remain complete dry) and submerge the wafer into the heated HCl solution and heat for 10 min.
11. Bring the beaker with the HCl solution together with the Si wafer remaining submerged and place under running DIW until the liquid is at about room temperature.
12. Repeat step 7 to rinse the Si wafer in fresh DIW for seven consecutive bathes.
13. Place the Si wafer on a spinner to spin-dry at 3000 rpm.
14. Place the dry Si wafer onto an Indium-free substrate holder and load into the vacuum chamber.

2.2 Growth Process

ZnTe growth was conducted using a MBE system, manufactured by DCA Instruments, equipped with a 3.25-in substrate heater. Three-inch Si(211) or Si(100) nominal wafers were used as substrates. Indium-free mounting was used to hold the Si wafer during growth. The modified RCA process was used to clean the Si wafers prior to growth (*24*). This process leaves an approximate 12 Å uniform oxide layer on the Si surface, which was easily thermally removed in the growth chamber at approximately 850 °C. After oxide removal, the Si substrates were cooled under As_4 flux to 400 °C. During the oxide desorption process, reflection high-energy electron diffraction (RHEED) patterns were used to monitor the Si surface. Desorption of oxide from the Si surface was indicated through the change of the RHEED patterns caused by the Si surface reconstruction. Finally, the sample was cooled to the nucleation temperature under Te flux, Zn flux, or no flux, depending on the experimental parameters of interest.

The growth of ZnTe was initiated with a seeding layer of thin ZnTe nucleated at approximately 300 °C on Si substrate, using migration-enhanced epitaxy (MEE) (*25*) with elemental Zn and Te sources, in which the Zn and Te cell shutter were alternately opened for 10 s, with a 10-s pause between each shutter opening. After nucleation, the seed layer was then annealed at 420 °C under Te flux for 10 min, followed by deposition of a thick (~6 μm) ZnTe layer onto the seed layer using a ZnTe compound source with additional Te or Zn or neither, depending on the experimental parameters of interest. The growth rate of ZnTe was approximately 0.6 μm/h. During ZnTe growth, the layer was periodically annealed at 460 °C under Te overpressure. This flash annealing improved both the ZnTe layer quality and the morphology of ZnTe layer. The temperature profile of this baseline MBE growth process is illustrated in figure 2. Our studies were focused on the substrate pretreatment prior to nucleation, as well as nucleation and growth temperatures of ZnTe and the II-VI flux ratio used during ZnTe growth. A retractable nude ion gauge was placed at substrate growth position prior to introducing the substrate to measure material fluxes. The measured values were used to determine the flux ratios used in this study.

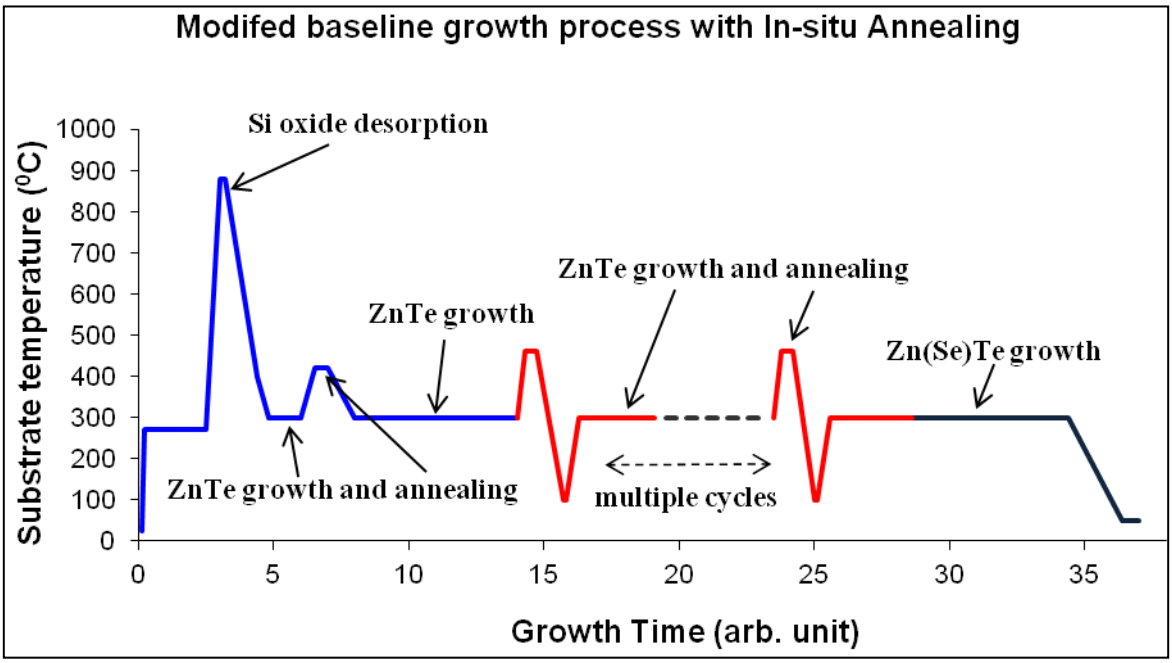

Figure 2. Temperature profile of baseline MBE growth process of Zn(Se)Te on Si.

2.3 Material Characterization

As-grown ZnTe/Si layers were evaluated by using a PANalytical X'pertProMPD X-ray diffractometer with a Cu Kα radiation (λ=1.5406 Å) and conventional θ–2θ X-ray diffraction (XRD) in order to gauge the overall crystalline quality. The surface morphologies of the as-grown layers were recorded using a phase contrast optical microscope equipped with a digital camera, and defect densities were related through direct observation and counting. To estimate the dislocation densities of the ZnTe/Si layers, a chemical decoration etch developed by Benson for CdTe and HgCdTe was used to reveal the dislocations (*26*). Although no direct link has yet been established, the etch pits are most likely associated with the dislocations generated during growth, considering the similarity between CdTe and ZnTe. These etch pits were observed and the etch pits density (EPD) was counted using an automated counting program that detects changes in grayscale due to pit presence against the non-pitted surface.

Thicknesses of the ZnSeTe/Si layers were estimated from interference fringes of IR transmission spectra, as shown in figure 3. Considering light passing through a thin film, the thickness (t) of the thin film can be expressed as a function of the interference fringe separation (Δ):

t (cm) = 1/(2nΔ), where n is the refraction index of the thin film.

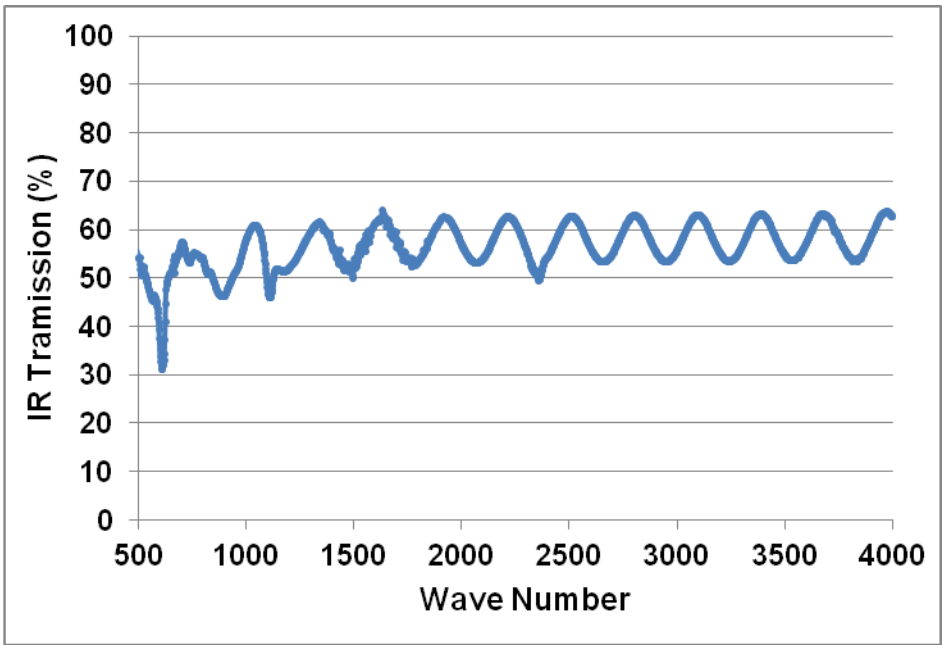

Figure 3. IR transmission spectrum of a ZnTe grown on Si(211).

3. Results and Discussion

3.1 Growth of ZnTe(211) on Si(211) – Growth Temperature Optimization

For MBE growth, it is well-established that growth temperature is one of the key parameters that dictates the quality and morphology of the epilayer. Since ZnTe was grown using a two-step growth process, both the nucleation temperature and growth temperature were optimized using X-ray full width at half-maximum (FWHM), surface morphology, and defect density (dislocations and micro defects). Experiments were designed with changes to only one variable at a time, and the MBE growths were carried out in consecutive runs.

Figure 4 shows the FWHM (right axis) of XRD from (422) planes and EPD (left axis) of as-grown ZnTe(211)/Si(211) layers as a function of the nucleation temperatures. All layers were nucleated at different temperatures between 260 and 360 °C using the MEE growth process with elemental Zn and Te, followed by a second growth fixed at 300 °C using a ZnTe compound source, which leads to a ZnTe(211)/Si layer of about 6 microns in thickness. The results indicate that the X-ray FWHM of the ZnTe/Si layer is not sensitive to the nucleation temperature, but the EPD defines an optimal growth window of about 280–320 °C. Similar relationships were found between surface morphology and nucleation temperature, as shown in figure 5, which is not quite sensitive to the nucleation temperature. The results are probably due to the self-terminated growth nature of the MEE growth process. Based on crystalline quality and surface morphologies of the ZnTe/Si layers nucleated at different temperatures, we concluded that a nucleation temperature of about 300 °C was optimal for ZnTe(211) grown on Si(211) by MBE.

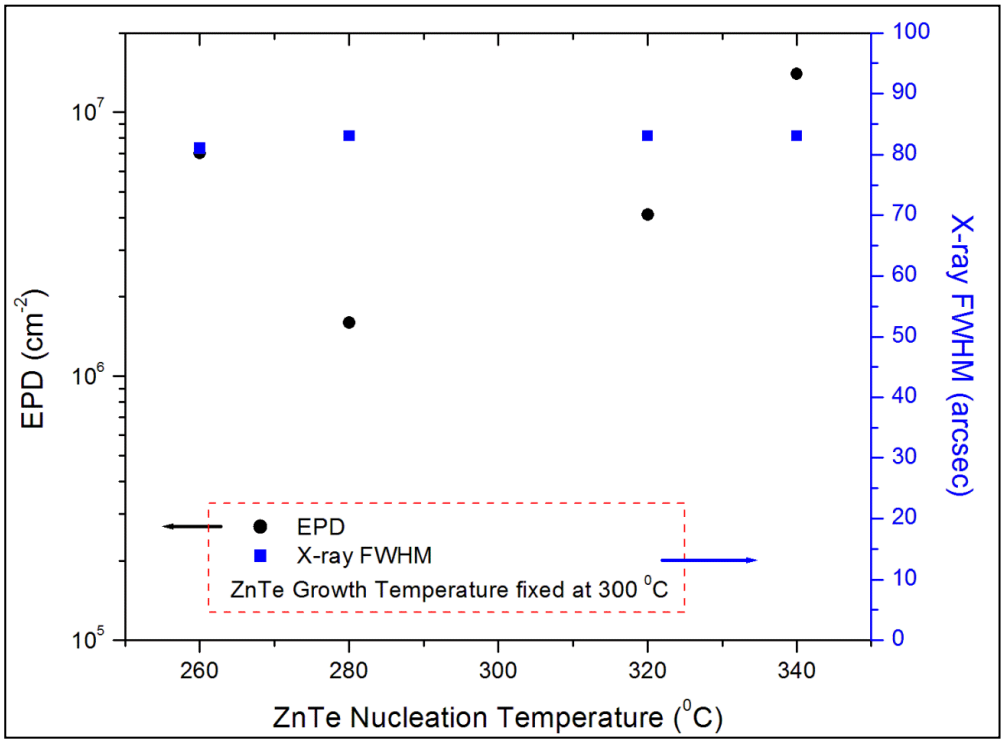

Figure 4. X-ray FWHMs (right axis) and EPD (left axis) of MBE as-grown ZnTe(211)/Si(211) layers as functions of nucleation temperatures.

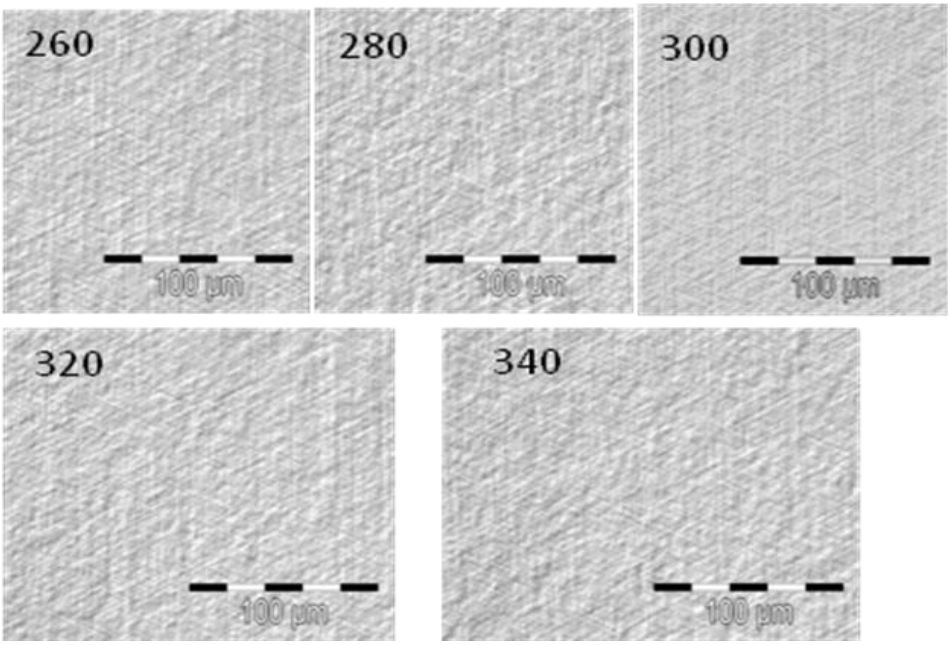

Figure 5. Surface morphologies of as-grown ZnTe(211)/Si(211) layers nucleated at different temperatures and grown at 300 °C.

After fixing the ZnTe nucleation temperature at 300 °C, the optimal growth temperature for the second step of the ZnTe growth was investigated. In this set of experiments, six ZnTe(211)/Si layers were nucleated at 300 °C using the MEE growth procedure, followed by growth of the thick ZnTe layer using different growth temperatures. The as-grown ZnTe/Si layers were then evaluated for their crystalline quality, as indicated by X-ray FWHM and dislocation density, shown in figure 6, and surface morphology, as shown in figure 7, as a function of growth temperature. The results clearly define an optimal growth window between 280 and 320 °C. Beyond this window, the ZnTe/Si layers exhibit much rougher surfaces and broader x-ray FWHM, which indicate deterioration of the crystalline quality. The surface roughening occurring at both the low end and high end of the growth window is probably due to lack of diffusivity at lower temperature, which promotes a disordered lattice arrangement, and a decrease of the sticking coefficient at higher temperature, which tends to lead to faceting. Since the facets for (211)-oriented crystals are mostly (111) planes, faceting will usually lead to formation of triangular shaped defects on the (211) surface. We observed that the defect count on these ZnTe(211)/Si wafers increases dramatically for growth at high temperatures, as shown in figure 8.

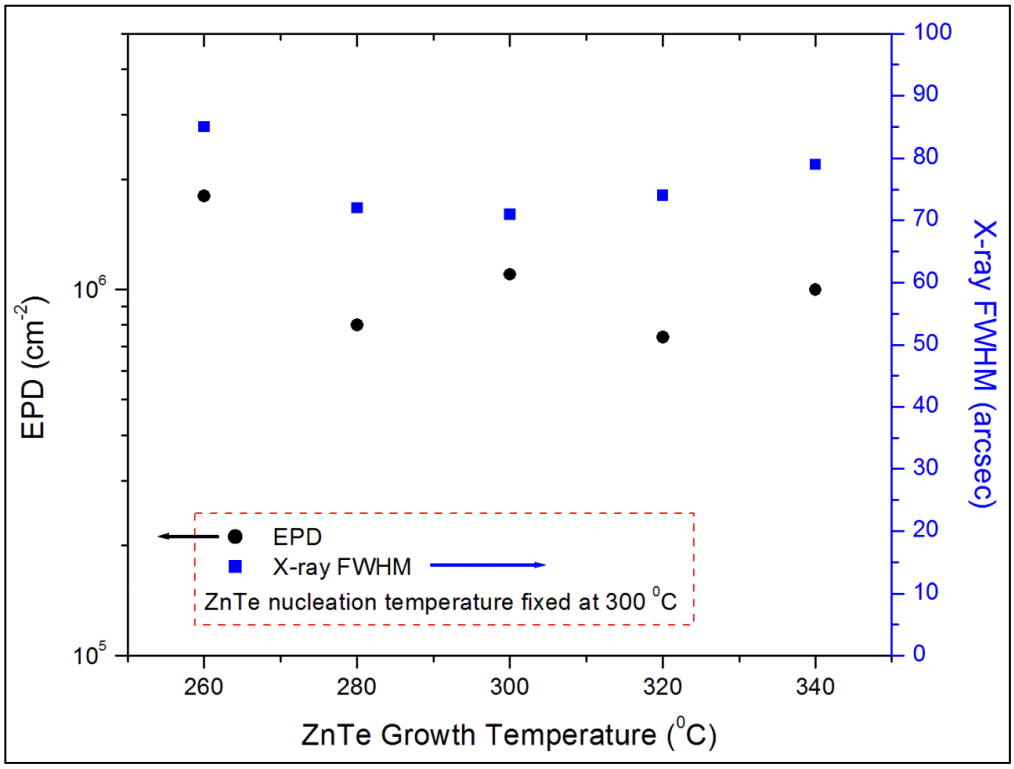

Figure 6. X-ray FWHMs (right axis) and EPD (left axis) of MBE as-grown ZnTe(211)/Si(211) layers as functions of growth temperatures.

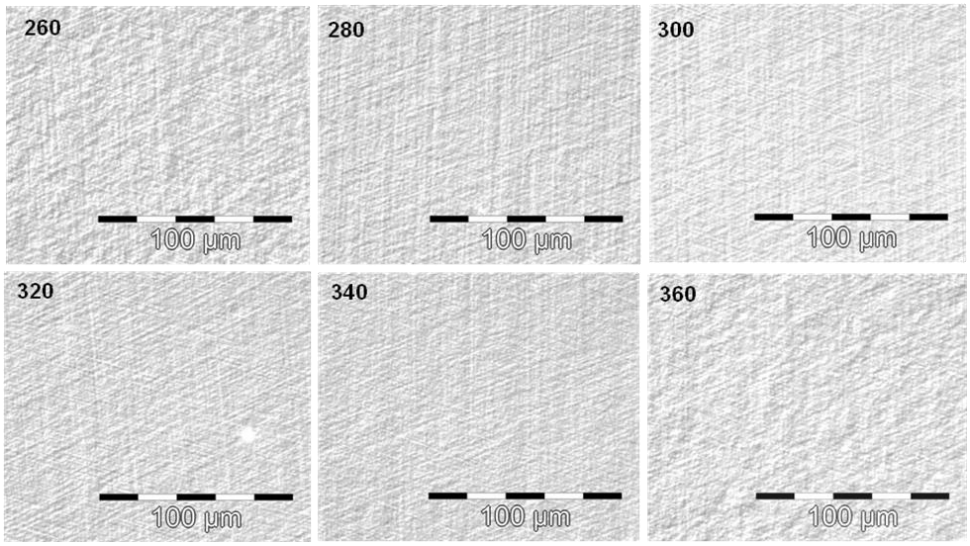

Figure 7. Surface morphologies of as-grown ZnTe(211)/Si(211) layers nucleated at 300 °C and grown at different temperatures.

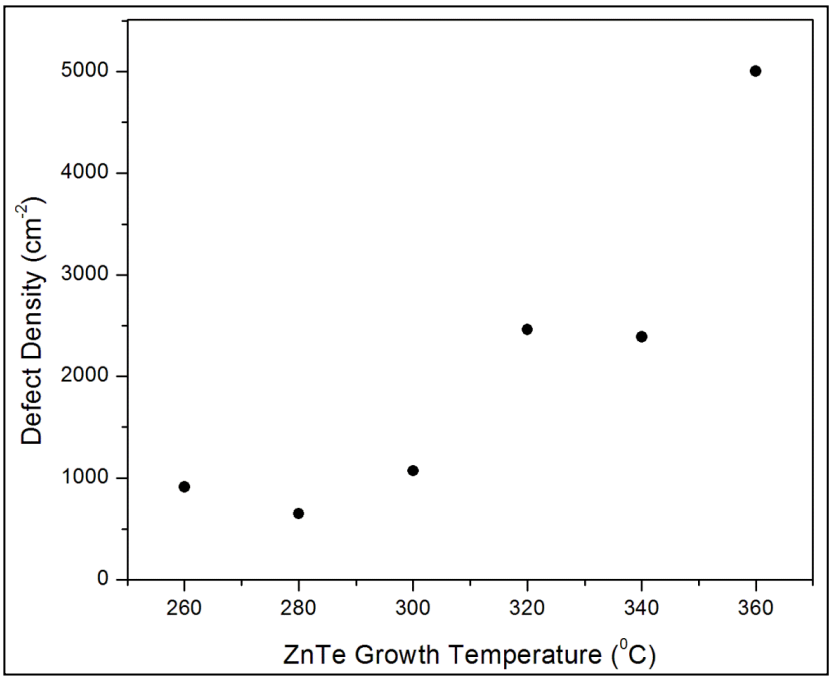

Figure 8. X-ray FWHMs of ZnTe/Si layers as a function of alloy composition.

3.2 Growth of ZnTe(211) on Si(211) – II/VI Flux Ratio Optimization

For heteroepitaxy of binary II-VI compounds, optimized growth conditions are usually achieved with certain ratio of II/VI compounds due to different desorption coefficients of group II and VI elements. In the case of ZnTe, which is a compound of period 3 (Zn) and period 4 (Te) in the Periodic Table, increased imbalance in the thermodynamic properties of Zn and Te probably leads to increased sensitivity of surface morphology and crystalline quality of ZnTe layer to the Zn/Te flux ratio. For heteroepitaxial growth of ZnTe(100) on III-V substrates, we found that the optimized growth conditions were achieved in Zn-rich growth environment (*27, 28*). In this investigation, we also studied the influence of the Zn/Te flux ratio on surface morphology and crystalline quality of ZnTe(211)/Si(211). All ZnTe layers were nucleated and grown at approximately 300 °C using the aforementioned growth procedures in three consecutive runs under three different II/VI flux ratios of 0.5, 1, and 2, respectively. X-ray FWHM (right axis) and EPD (left axis), as well as surface morphologies of these three ZnTe(211)/Si layers, are shown in figure 9.

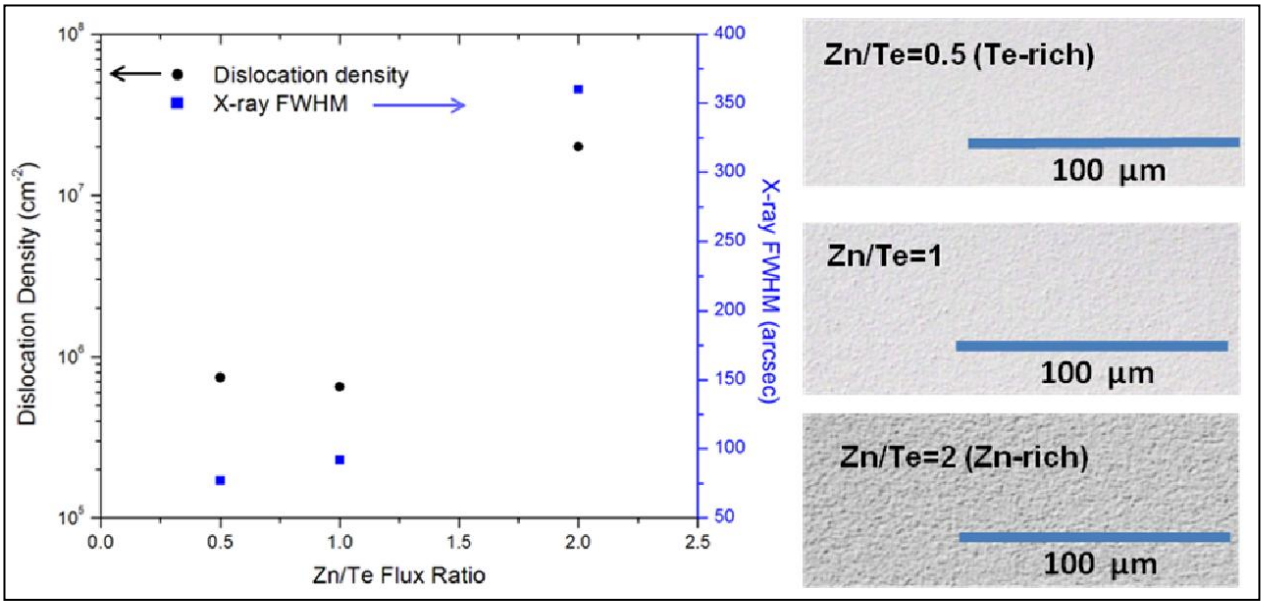

Figure 9. X-ray FWHMs (right axis) and EPD (left axis) as well as surface morphologies (right) of as-grown ZnTe(211)/Si(211) layers nucleated and grown at 300 °C with different Zn/Te ratios.

The results indicate that ZnTe(211)/Si layers of much better quality were obtained when grown under either Te-rich or equal Te and Zn fluxes, which is opposite to the results obtained from ZnTe(001) grown on III-V substrates under Zn-rich environment. In our case, ZnTe(211) layers grown under a Zn-rich environment, exhibit, without exception, a very hazy surface morphology visible even to the unaided eye and very broad x-ray FWHM—a factor of 4 higher than that of the layers grown under Te-rich conditions.

The inferior material quality of ZnTe(211) grown under Zn-rich conditions is further evidenced by cross-section transmission electron microscopy (TEM) images, such as those shown in figure10a. The high density of lamellar-twinned defects present is clearly the main defect responsible for the inferior crystallinity observed by x-ray diffraction and EPD etching. In contrast, ZnTe(211) layers grown either under Te-rich or a 1:1 flux ratio exhibit very smooth and orderly interfacial structure, as illustrated in figure 10b. The Fourier-filtered high resolution TEM image clearly exhibits an array of misfit dislocations present at the ZnTe/Si interface, as indicated by the arrows, with separations that correspond to the 12% lattice mismatch between ZnTe and Si.

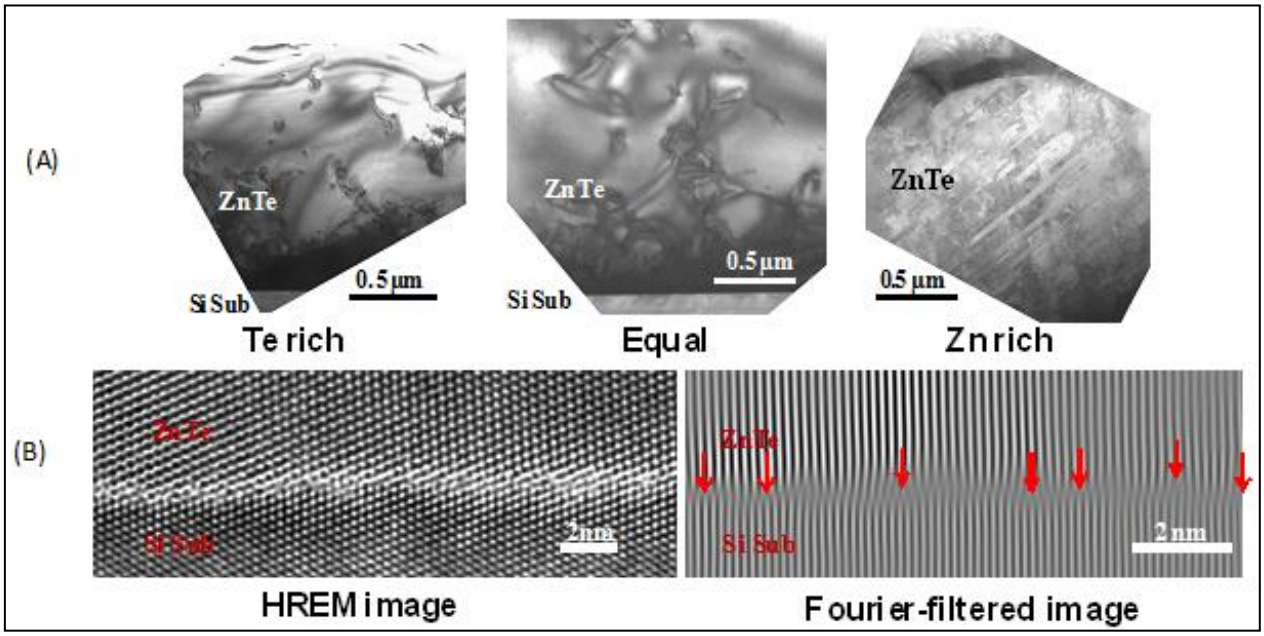

Figure 10. Cross-section TEM images of as-grown ZnTe(211)/Si(211) layers nucleated and grown at 300 °C with different Zn/Te ratios (A) and high resolution TEM images (B, left) and Fourier-filtered image (B, right) of ZnTe/Si interface of the ZnTe(211)/Si(211) layers grown under Te-rich conditions.

3.3 Growth ZnTe(100) on Si(100)

Since ZnTe/Si can be regarded as a potential alternate substrate for T2-SLS, which are currently grown on GaSb(100) substrates, it is desirable to develop a baseline growth process for ZnTe(100)/Si(100). Although there are some limited studies on the MBE growth of ZnTe(100) on GaAs as well as other III-V substrates, growth of ZnTe(100) on Si(100) has received hardly any attention in the past. Based on some similarities between ZnTe(211)/Si and ZnTe(100)/Si, this study started by utilizing the optimized growth parameters for ZnTe(211)/Si(211) and, thus, focused on the impact of pre-nucleation treatment prior to ZnTe nucleation and the Zn/Te flux ratio during ZnTe growth, on surface morphology, and crystalline quality.

For any heteroepitaxial system, in particular a system with a polar material such as ZnTe(100) on a non-polar substrate such as Si(100), establishing an appropriate epitaxial template is critical for determining quality of the epilayer. For this reason, we investigated pre-nucleation treatment of the Si(100) surface with either a Te flux, a Zn flux, or no flux, and the impact on the epilayers. Three consecutive MBE runs were carried out under identical growth conditions to grow ZnTe(100) layers on Si(100) substrates pre-treated with Zn, Te or neither, respectively, prior to ZnTe nucleation. The as-grown ZnTe(100)/Si(100) wafers were then evaluated, and the results are illustrated in figure 11. The x-ray FWHM (left) and surface morphology (right) clearly indicate that ZnTe(100) grown on Si(100) with either Zn or no pretreatment exhibits a very rough surface and poor crystalline quality. On the other hand, ZnTe(100) grown with the Te

pretreatment shows much smoother surface and better quality. However, the ZnTe exhibits a surface morphology that is dominated by dense and characteristic hillock structures, which indicates that the growth conditions are still far from optimized.

In similar fashion, we studied the impact of Zn/Te flux ratio during ZnTe growth. In this case, three ZnTe(100) layers were grown consecutively at 300 °C on Si(100) substrate and pretreated with Te prior to the ZnTe nucleation, but under three different Zn/Te flux ratios during the ZnTe growth. Figure 12 shows the x-ray FWHM (left) and surface morphology (right) of the three ZnTe(100) layers as functions of the Zn/Te flux ratio, which leads to the conclusion that better ZnTe(100) layers have to be grown under Zn-rich conditions. Our results are in line with other reports for ZnTe(100) layers grown on other III-V substrates (*27*, *28*). However, more work is clearly needed to determine the degree of Zn-rich conditions, as well as optimized growth temperatures for ZnTe(100) on Si(100), in order to achieve the highest possible quality of ZnTe(100)/Si(100) and eventually ZnSeTe(100)/Si(100) wafers.

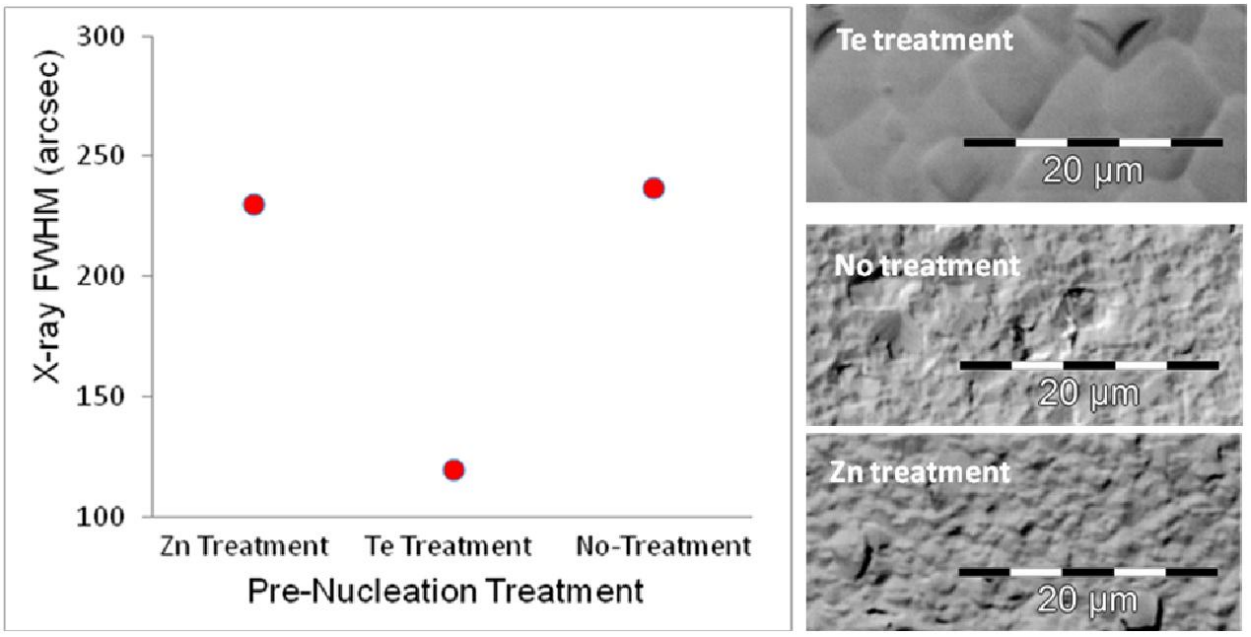

Figure 11. X-ray FWHMs (left) and surface morphologies (right) of as-grown ZnTe(100)/Si(100) layers nucleated and grown at 300 °C with different pre-nucleation treatments.

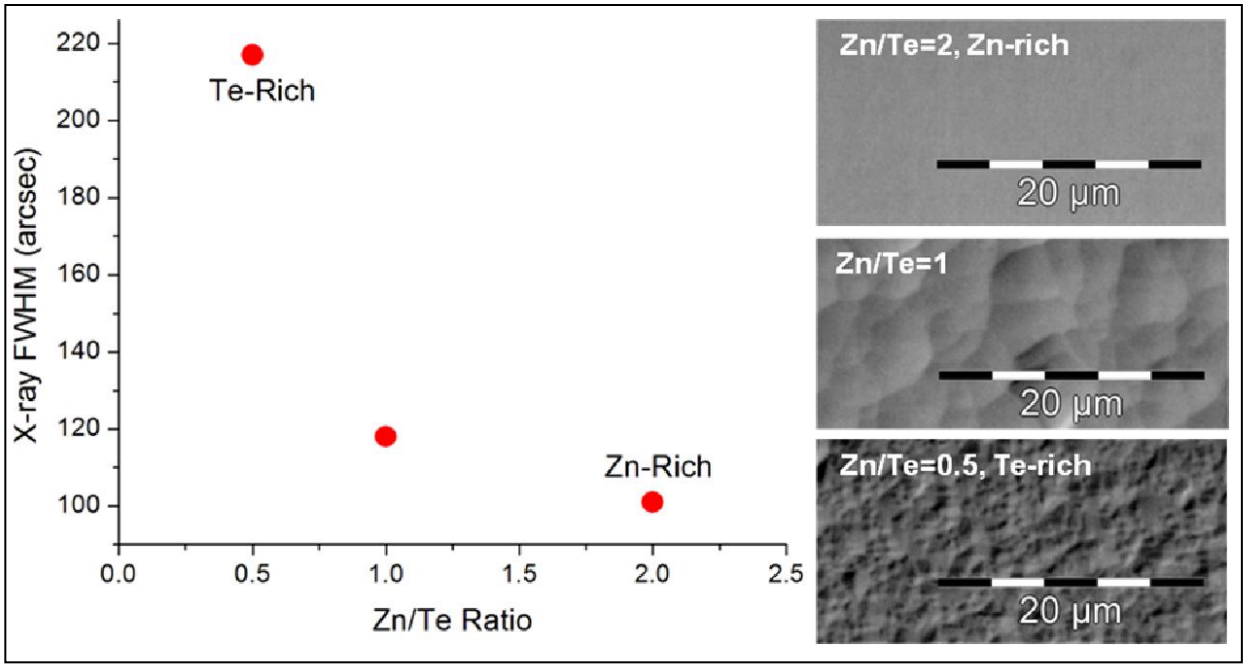

Figure 12. X-ray FWHMs (left) and surface morphologies (right) of as-grown ZnTe(100)/Si(100) layers nucleated and grown at 300 °C under different Zn/Te flux ratios.

4. Conclusions

We have reported the MBE growth of ZnTe on Si substrates in both (211) and (100) orientations. The best ZnTe(211) layers were nucleated and grown at about 300 °C and under Te-rich conditions on Si(211) substrates, whereas the best ZnTe(100) layers were grown at about 300 °C and under Zn-rich conditions on Si(100) substrates pretreated with Te prior to the ZnTe nucleation. Near optimal growth procedures have been established for MBE growth of ZnTe on Si with high crystalline quality, low defect, and dislocation densities, as well as excellent surface morphology. Using this baseline MBE growth process, we are able to obtain ZnTe(211)/Si wafers with X-ray FWHM as low as 70 arcsec, low EPD, and defect density.

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List of symbol, Abbreviation, and Acronyms

BEP	beam equivalent pressure
DIW	de-ionized water
EPD	etch pits density
FPAs	focal plane arrays
FWHM	full width at half-maximum
H_2O_2	hydrogen peroxide
HCl	hydrogen chloride
HF	hydrogen fluride
IR	infrared
IRFPA	IR focal-plan array
LWIR	long wavelength infrared
MBE	molecular beam epitaxy
MEE	migration-enhanced epitaxy
MWIR	medium wavelength infrared
NH_4OH	ammonium hydroxide
RHEED	reflection high-energy electron diffraction
SWIR	short wavelength infrared
T2-SLS	type-II strained layer superlattices
TEM	transmission electron microscope
XRD	x-ray diffraction

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